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| EXAMINER | |
|---|---|
| RADOSEVICH, STEVEN D | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2138 | |

DATE MAILED: 10/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/806,093 | GUETTAF, AMAR | |
| | Examiner | Art Unit | |
| | Steven D. Radosevich | 2138 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *8 and 21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-20 and 22-28* is/are rejected.

7)☒ Claim(s) *4 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

- 1.☐ Certified copies of the priority documents have been received.
- 2.☐ Certified copies of the priority documents have been received in Application No. _____.
- 3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

Claims 1-28 are present for examination. Acknowledgement is made that claims 8 and 21 have been cancelled without prejudice and as such will not receive any further consideration within this examination of the remaining claims within the instant application presented to the office.

### *Drawings*

The drawings at this time are not objected to, since there do not seem to be any further issues that would require an objection. As such the drawings as submitted to the office on 8/18/2006 are accepted.

### *Claim Objections*

The claim objection(s) not addressed by the applicant are being maintained since appropriate corrections were not made nor did the applicant provide explanation as to why corrections were not made to the claim(s) while the issues still exist.

Claims 4 and 20 are objected to because of the following informalities:

There is a grammatical error in line 2 of each claim. For purposes of examination Examiner interprets that scan tests are conducted "on" not "for" the plurality of scan paths.

Appropriate correction is required.

Acknowledgement is made that the applicant has overcome the other claim objections stated within the initial examination of the instant application via correction or explanation. At this time there does not appear to be any other claim objection other

then those indicated above. Applicant is asked to correct the claims or provide explanation as to why corrections will not be made.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-7, 9-16, 17-20, and 22-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 1 and 17 the issue pertaining to the segmentations/segment point serving no purpose in the invention as it has been claimed still is present within step (f) or (g) respectfully of the claims. As it was stated within the previous examination, the scan paths, all the scan paths in this step (step (f) or (g) respectfully) are examined in their entirety, which leaves it unclear to the Examiner as to how a shifting of the segment point is performed within this step (step (f) or (g) respectfully).

Examiner notes that in the previous step (e) or (f) respectfully the segmented portion following the segment point is examined and used in the tracing of the source of errors when meeting the claimed criteria while the preceding segmented portion to the segment point was left out of examination. Examiner suggested that the applicant make an indication as done in step (e) or (f) respectfully as to which segmented segment is examined and used to determine the shifting. The Examiner's understanding that only the segmented segment following the segment point in step (e) or (f) respectfully is examined and used in the tracing of the source of errors within that segment when

meeting the claimed criteria while the preceding segmented portion to the segment point was left out/ignored of examination and tracing is attributed to the applicant's amendment to step (e) or (f) respectfully within is instant claims presented to the office.

Further, as per claims 1 and 17 it is unclear to the examiner how any of the "other scan paths within the plurality of scan paths . . . considered to be good scan paths" after being tested along with the identified "bad scan path" can have test results that effect the tracing and shifting within the identified "bad scan path." The Examiner interprets that the number of errors within any of the "other scan paths" resulting in the segment point shifting results in the segment point shifted completely to either end of the "bad scan path," resulting in a never ending loop of shifting, negating tracing to take place within the segment of the "bad scan path" that follows the segment point as understood by the Examiner. The same applies to the tracing as has been just described for the shifting.

Claims 2-7, 9-16, 18-20, and 22-28 are dependent upon independent claims 1 and 17 respectfully and therefor inherit the 35 USC § 112-second paragraph issues and may not be further considered on their merits.

Acknowledgement is made that the applicant has overcome the other claim 35 USC § 112-second paragraph rejections stated within the initial examination of the instant application via correction. At this time there does not appear to be any other claim 35 USC § 112-second paragraph rejections other then those indicated above. Applicant is asked to correct the claims or provide explanation for understanding.

***Response to Arguments***

Applicant's arguments filed 8/18/2006 have been fully considered by the Examiner. Applicant's arguments with respect to claims 1-7, 9-20, and 22-28 have been considered but are moot in view of the new ground(s) of rejection in view of Martin-de-Nicolas et al (U.S. Publication 2003/0208710) in view of Applicants Admitted Prior Art (AAPA) used in the initial examination and non-final Office Action of the instant application mailed to Applicant on 04/18/2006.

Applicant argues the following with respect to the claims 1-7, 9-20, and 22-28:

i. The references cited do not teach, disclose or suggest the element of:

(1) Shifting the segment point based on an analysis of the error generated by the bad scan path and the good scan paths and returning to step (b) when the number of errors of an output of the bad scan path are greater than a bad scan path error threshold or the number of errors on an output of any one of the good scan paths is greater than a good path error threshold.

As per applicant's argument (i), the Examiner would like to direct applicant to the issue of claim 17 not having the shifting step, which is identified as the believed patentable limitation not taught, disclosed or suggested within the referenced art cited identically identified as in claim 1. The Shifting step of claim 17 is step (g) not step (f) as indicated in the argument within the instant response from applicant. For the purposes

of this examination the element not believed to be taught, disclosed or suggested within the referenced art cited with respect to claim 17 will be step (g).

Further as per applicant's argument (i), the Examiner would like to direct the applicant to the AAPA specifically paragraphs 0003 and 0005 of the instant application. The applicant indicates, "The sheer number of flip-flops within an integrated circuit, which is often greater than a million, presents a daunting challenge for testing." The applicant further indicates, "While scan testing provides significant benefits, a shortcoming exists related to efficiently debugging a scan testing failure to identify the source or sources of the failure."

In the instant response from the applicant, the applicant indicates and acknowledges on page 14 that Martin-de-Nicolas discloses, "reducing the number of instructions . . . when there is a test error to help determine what instruction is causing the error." Those of ordinary skill in the art at the time the invention was made would recognize that a "bug" is equivalent terminology with an "error" in the art.

Those of ordinary skill in the art at the time the invention was made would find a motivation to combine prior art references (those used in the initial examination and non-final Office Action of the instant application) in the nature of the problem being solved. **Ruiz v. A.B. Chance Co.,** 357 F.3d 1270, 1276, 69 USPQ2d, 1686, 1690 (Fed. Cir. 2004); also **Pro-Mold & Tool Co. v. Great lake Plastic Inc.,** 75 F.3d 1568, 1573, 37 USPQ2d 1626, 1630; **In re Huang**, 100 F.3d 135, 139 n.5; 40 USPQ2d 1685, 1688 n.5 (Fed. Cir. 1996). Martin-de-Nicolas teaches a "binary search algorithm" used to "quickly identify the failing instruction" after testing a DUT in paragraph 0029. Those of

ordinary skill in the art at the time the invention was made would recognize that the sheer number of instructions required to test a DUT may be greater than a million, presenting a daunting challenge for testing and identifying the source or sources of failure. AAPA teaches that millions of flip-flops within a DUT present a daunting challenge for testing and efficiently debugging a scan testing failure to identify the source or sources of failure as indicated above. Martin-de-Nicolas is directed to solving the problem of quickly identifying the failure(s) within a test that presents a great multitude of locations wherein the failure(s) may exist. The Examiner finds that the nature of the problem to be solves also provides more than sufficient motivation to combine the prior art references.

Finally Applicant is reminded that the M.P.E.P. (see M.P.E.P. 2111) requires that the examiner give "the broadest reasonable interpretation" of the claims "consistent with the specification." It also warns that "reading a claim in light of the specification, to thereby interpret limitations explicitly recited in the claim, is a quite different thing from reading limitations of the specification into a claim, to thereby narrow the scope of the claim by implicitly adding disclosed limitations which have no express basis in the claim." The claims must stand on their own.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-7, 10, 20, and 22-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin-de-Nicolas et al (U.S. Publication 2003/0208710) in view of Applicants Admitted Prior Art (AAPA) as described above and as follows in some detail.

2. As per claim 1, Martin-de-Nicolas teaches scan testing of an integrated circuit with a plurality of scan paths, a method of debugging scan testing failures of the integrated circuit, comprising the steps of:

b. Identifying a bad scan path that is generating one or more errors within the plurality of scan paths (0019 lines 7-9 in addition to 0022 lines 15-19);

c. Defining a segment point that segments the bad scan path into two segments (0028-0031);

d. Conducting scan tests on the plurality of scan paths (0019 line 9)

e. Assessing scan test results on the bad (0018 lines 8-10 and 0022 lines 16-19);

f. Tracing the source of errors when the number of errors of an output of the bad scan path following the segment point are less than a bad path error threshold (0018 lines 10-12 and 0029); and

g. Shifting the segment point based on an analysis of the errors generated by the bad scan path and the good scan path and returning to step (b) when the number of errors of an output of the bad scan path are greater then a bad path error threshold (0028-0029 and 0031).

Martin-de-Nicolas does not specifically teach wherein in step (a) all other scan paths within the plurality of scan paths are considered to be good scan paths.

However as noted within the AAPA in paragraph 0005 "when there is a failure within a particular scan path, errors will be generated on the output of that scan path [bad scan path], but also can be propagated to other scan paths [good scan paths] through logical and physical interconnections." Therefore those of ordinary skill in the art at the time the invention was made would recognize that scan chains that produce an error at their output may have produced the errors not because they are bad scan paths but because of their logical and physical interconnections with a bad scan path which produces the error(s).

Therefore those of ordinary skill in the art at the time the invention was made would have been motivated within the method of Martin-de-Nicolas to select a single scan path outputting an error(s) from a number of scan paths outputting an error(s) to be a "bad scan path," while all others are presumed to be "good scan paths," to examine the "bad scan path" with the described binary search method in Martin-de-Nicolas so as to quickly determine if that scan path is the scan path producing the error(s) in other scan paths by quickly identifying the faulty location(s) within that scan path and fix, replace, or bypass the faulty circuitry, thus eliminating the error(s)

produced within that san path ("bad scan path") and/or other scan paths ("good scan paths") that only through "logical and physical interconnections with" that bad scan path may output an error(s) which would save time and money since each scan path outputting an error(s) does not need to be examined.

3. As per claims 2 and 18, Martin-de-Nicolas teaches that all the scan paths are tested a number of times with multiply tests confirming which scan paths are faulty and which are not (0019 line 7-9 in addition to 0022 lines 15-19).

4. As per claims 3 and 19, the art is replete with masking of identified faulty scan paths while further testing any remaining unidentified scan paths as faulty with various tests. This method of masking reduces processing time since the identified faulty scan paths are not retested or examined since they are already found to be faulty (0019 lines 7-9).

5. As per claim 4, Martin-de-Nicolas teaches wherein step (a) of claim 1 includes running a series of scan tests for the plurality of scan paths (0019 lines 7-9 in addition to 0022 lines 15-19).

6. As per claims 5-7, Martin-de-Nicolas teaches the above as per claim 1 wherein a number of testes are executed on a plurality of scan paths (0019 lines 7-9 with in addition to 0022 lines 16-19).

Martin-de-Nicolas does not specifically teach wherein these tests executed include varying the temperature of the integrated circuit, frequency of a clock signal input, or the test voltage.

However, as evidenced by the AAPA within the specification of the instant application it was known at the time the invention was made when factors such as frequency, temperature, or voltage are changed, errors within that circuit can be caused (0006).

7. Therefore, the Examiner interprets that the plurality of tests run by Martin-de-Nicolas incorporates these factors of varying the temperature, frequency, and test voltage, wherein these factors are within the limitations in which the circuit is rated to operate since Martin-de-Nicolas desires as does the applicant to identify and locate errors within a DUT (0008, 0019 lines 7-9 with 0029 lines 5-9).

8. As per claims 10 and 22, Martin-de-Nicolas teaches wherein in step (e) of claim 1 and (f) ("I" in this examination) the tracing of errors includes identifying a first error source that generated an error and determining whether the error originated with the first error source (0029). Examiner interprets that "identifying a first error source," is the determining of the location of the error, that error must have originated within "the first error source," since it was identified as the first error source.

9. As per claims 11 and 23, Martin-de-Nicolas teaches wherein the tracing the source of errors is conducted manually (0005 lines 1-3).

10. As per claims 12 and 24, Martin-de-Nicolas teaches wherein the tracing the source of errors is conducted automatically through an automated testing unit (0008).

11. As per claims 13-16 and 25-28, Martin-de-Nicolas teaches the sifting of the segment point midway or in the direction from its present location to the end/beginning of the scan chain dependent on the testing results (0028-0029 and 0031). Examiner

notes that this is the implementation of a binary search for locating errors or faults such as taught throughout the publication by Martin-de-Nicolas.

12. As per claim 17, Martin-de-Nicolas teaches scan testing of an integrated circuit with a plurality of scan paths, a method of debugging scan testing failures of the integrated circuit, comprising the steps of:

h. Identifying a plurality of bad scan paths that is generating one or more errors within the plurality of scan paths (0019 lines 7-9 in addition to 0022 lines 15-19);

i. Masking all bad scan paths except a bad scan path under test (0019 lines 7-9);

j. Defining a segment point that segments the bad scan path into two segments (0028-0031);

k. Conducting scan tests on the plurality of scan paths (0019 line 9);

l. Assessing scan test results on the bad (0018 lines 8-10 and 0022 lines 16-19);

m. Tracing the source of errors when the number of errors of an output of the bad scan path under test are less than a bad path error threshold (0018 lines 10-12 and 0029);

n. Shifting the segment point based on an analysis of the errors generated by the bad scan path and the good scan path and returning to step when the number of errors of an output of the bad scan path under test are greater then a bad path error threshold (0028-0029 and 0031); and

o. Repeating steps (b) ("i" in this examination) through (g) ("n" in this examination) until the source or sources of errors within all dad scan paths among said plurality of bad scan paths have been located 0033 lines 6-8).

Martin-de-Nicolas does not specifically teach wherein in step (a) all other scan paths within the plurality of scan paths are considered to be good scan paths.

However as noted within the AAPA in paragraph 0005 "when there is a failure within a particular scan path, errors will be generated on the output of that scan path [bad scan path], but also can be propagated to other scan paths [good scan paths] through logical and physical interconnections." Therefore those of ordinary skill in the art at the time the invention was made would recognize that scan chains that produce an error at their output may have produced the errors not because they are bad scan paths but because of their logical and physical interconnections with a bad scan path which produces the error(s).

Therefore those of ordinary skill in the art at the time the invention was made would have been motivated within the method of Martin-de-Nicolas to select a single scan path outputting an error(s) from a number of scan paths outputting an error(s) to be the "bad scan path," while all others are presumed to be "good scan paths" or masked, to examine the "bad scan path" with the described binary search method in Martin-de-Nicolas so as to quickly determine if that scan path is the scan path producing the error(s) in other scan paths by quickly identifying the faulty location(s) within that scan path and fix, replace, or bypass the faulty circuitry, thus eliminating the error(s) produced within that san path ("bad scan path") and/or other scan paths ("good scan

paths") that only through "logical and physical interconnections with" that bad scan path may output an error(s) which would save time and money since each scan path outputting an error(s) does not need to be examined.

13. As per claim 20, Martin-de-Nicolas teaches wherein step (a) of claim 17 ("g" in this examination) includes running a series of scan tests for the plurality of scan paths (0019 lines 7-9 in addition to 0022 lines 15-19).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Martin-de-Nicolas (2003/0208710) in view of AAPA as applied to claim 1 above, and further in view of Akita (5541940) or Sugimoto et al. (6999386).

14. As per claim 9, Martin-de-Nicolas teaches the above as per claim 1 wherein a binary search is performed to locate the error or failure.

Martin-de-Nicolas does not specifically teach wherein in step (d) there is included a determination of the number of errors generated by the bad scan path following the segment point and each of the good scan paths.

However in the analogous arts of both Akita and Sugimoto it is taught that it is important to determine the number of errors generated from a DUT.

Therefore, one of ordinary skill in the art at the time the invention was made would have been motivated to combine the binary search as taught by Martin-de-Nicolas by adding to it determining of the number of errors generated by a DUT as taught by either Akita or Sugimoto so that a determination of weather or not the number of errors exceeds the capacity of the system may be made and so that all detected errors are located if the number of errors falls within the capacity of the system to do so.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

ii. Bhavsar et al. (U.S. Patent 6260166) discloses a binary search in an efficient production test and debug architecture.

iii. Wilson et al. (U.S. Patent 5210486) discloses a binary search within a circuit test method.

iv. Koo et al. (U.S. Patent 5386423) discloses a binary search used within testing.

v. Lindberg et al. (U.S. Patent 5663967) discloses a binary search used within scan-path testing and probing.

vi. Klaiber et al. (U.S. Patent 5905855) discloses a binary search used to rapidly narrow the search for an error.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven D. Radosevich
Examiner
Art Unit 2138

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